PENDING CLAIMS AS AMENDED

1. (currently amended) An encoding method for reducing decoding complexity, the method comprising:

encoding systematic bits in each of a plurality of buffers with a first code;

multiplexing content of the plurality of buffers; and

encoding said multiplexed content with [[as]] a second code to provide a set of frames.

2. (currently amended) The method as claimed in claim 1 wherein said encoding systematic bits in each of [[a]] the plurality of buffers with [[an]] the first code comprises:

encoding systematic bits in each of the plurality of buffers with a block code.

3. (currently amended) The method as claimed in claim [[1]] 2 wherein said encoding systematic bits in each of [[a]] the plurality of buffers with a block code comprises:

encoding systematic bits in each of the plurality of buffers with a Reed-Solomon code.

4. (original) The method as claimed in claim 1 wherein said multiplexing content of the plurality of buffers comprises:

providing a block of bits successively from each of the plurality of buffers.

5. (currently amended) The method claimed in claim 4 wherein said providing [[a]] the block of bits successively from each of the plurality of buffers comprises:

providing [[a]] the block of bits comprising a row of each of the plurality of buffers.

6. (currently amended) The method claimed in claim 1 wherein said encoding said multiplexed content with [[an]] the second code to provide [[a]] the set of frames comprises:

identifying a block of bits to be encoded; and

encoding the block of bits with [[a]] the second code.

7. (currently amended) The method claimed in claim 6 wherein said identifying [[a]] the block of bits to be encoded comprises:

identifying [[a]] the block of bits received from [[a]] at least one of the plurality of buffers.

8. (currently amended) A method reducing decoding complexity, comprising:

decoding received frames by [[an]] a second decoder;

de-multiplexing correctly decoded frame to a plurality of buffers; and

processing content of each of the plurality of buffers.

9. (currently amended) The method as claimed in claim 8 wherein said de-multiplexing correctly decoded frame to [[a]] the plurality of buffers comprises:

identifying a block of bits belonging to[[a]] at least one of the plurality of buffers; and

providing the block of bits to the buffer.

10. (currently amended) The method as claimed in claim 9 wherein said identifying [[a]] the block of bits belonging to [[a]] at least one of the plurality of buffers comprises:

identifying [[a]] the block of bits comprising a frame decoded by the second decoder.

11. (original) The method as claimed in claim 8 wherein said processing content of each of the plurality of buffers comprises:

providing systematic portion of each of the plurality of buffers to higher layers.

12. (currently amended) The method as claimed in claim 3 further comprising:

providing indication of an erasure to [[a]] the second decoder communicatively coupled to [[the]] at least one of the plurality of buffers that would receive the correctly decoded frame if the frame failed to decode correctly.

13. (currently amended) The method as claimed in claim 12 wherein said processing content of each of the plurality of buffers comprises:

decoding the systematic portion of the buffer by [[a]] the second decoder when the systematic portion is recoverable; and

providing the systematic portion of each of the plurality of buffer to higher layers.

14. (currently amended) A method for reducing decoding complexity, comprising:

encoding systematic bits in each of a plurality of transmit buffers with [[an]] a first code;

multiplexing content of the plurality of transmit buffers;

encoding said multiplexed content with [[an]] a second code to provide a set of frames;

transmitting the set of frames;

decoding received frames by [[an]] a second decoder;

de-multiplexing correctly decoded frame to a plurality of receive buffers; and

processing content of each received buffer.

15. (currently amended) The method as claimed in claim [[16]] 14 wherein said encoding systematic bits in each of [[a]] the plurality of transmit buffers with [[an]] a first code comprises:

encoding systematic bits in each of [[a]] the plurality of transmit buffers with a block code.

16. (currently amended) The method as claimed in claim 15 wherein said encoding systematic bits in each of [[a]] the plurality of buffers with [[a]] the block code comprises:

encoding systematic bits in each of a plurality of buffers with a Reed-Solomon code.

17. (currently amended) The method as claimed in claim 14 wherein said multiplexing content of the plurality of the [[first]] transmit buffers comprises:

providing a block of bits successively from each buffer.

18. (currently amended) The method claimed in claim 17 wherein said providing [[a]] the block of bits successively from each buffer comprises:

providing [[a]] the block of bits comprising a row of [[the]] at least one of the plurality of transmitting buffers.

19. (currently amended) The method claimed in claim 14 wherein said encoding said multiplexed content with [[an]] the second code to provide [[a]] the set of frames comprises:

identifying a block of bits to be encoded; and

encoding the block of bits with [[an]] the second code.

20. (currently amended) The method claimed in claim 19 wherein said identifying [[a]] the block of bits to be encoded comprises:

identifying the block of bits as [[a]] the block of bits received from [[a]] at least one of the plurality of transmit buffers.

21. (currently amended) The method as claimed in claim 14 wherein said de-multiplexing correctly decoded frame to a receive buffers comprises:

identifying a block of bits belonging to [[a]] at least one of the plurality of receive buffers; and

providing the block of bits to [[the]] at least one of the plurality of receive buffers.

22. (currently amended) The method as claimed in claim 21 wherein said identifying [[a]] the block of bits belonging to [[a]] at least one of the plurality of receive buffers. comprises:

identifying [[a]] the block of bits as a block of bits comprising a frame decoded by the second decoder.

23. (original) The method as claimed in claim 14 wherein said processing content of each receive buffer comprises:

providing systematic portion of each buffer to higher layers.

24. (currently amended) The method as claimed in claim 14 further comprising:

providing indication of an erasure to [[an]] a first decoder communicatively coupled to the receive buffer that would receive the correctly decoded frame if the frame failed to decode correctly.

25. (currently amended) The method as claimed in claim 24 wherein said processing content of each buffer comprises:

decoding the systematic portion of [[the]] at least one of the plurality of receive buffers by [[an]] the first decoder when the systematic portion is recoverable; and

providing systematic portion of each buffer to higher layers.

26. (original) An apparatus for reducing decoding complexity, comprising:

a plurality of buffers;

a plurality of encoders, each of said plurality of encoders being communicatively coupled to one of said plurality of buffers;

a multiplexer communicatively coupled to said plurality of buffers; and

an inner encoder communicatively coupled to said multiplexer.

27. (original) The apparatus as claimed in claim 26 wherein each of said plurality of buffers is configured to:

store systematic bits and parity bits.

28. (currently amended) The apparatus as claimed in claim 26 wherein [[each of]] each of said plurality of encoders is configured to:

encode systematic bits to provide parity bits.

29. (original) The apparatus as claimed in claim 28 wherein each of said plurality of encoders is configured to:

encode the systematic bits with a block code.

30. (currently amended) The apparatus as claimed in claim 26 wherein [[each of]] each of said plurality of encoders is configured to:

encode the systematic bits with a Reed-Solomon code.

31. (original) The apparatus claimed in claim 26 wherein said multiplexer is configured to:

provide a block of bits successively from each of said plurality of buffers to said inner encoder.

32. (original) The apparatus as claimed in claim 31 wherein said block of bits comprises a row of said buffer.

33. (original) The apparatus as claimed in claim 26 wherein said inner encoder is configured to:

identify a block of bits to be encoded; and

encode the block of bits with an inner code.

34. (original) The apparatus as claimed in claim 33 wherein said block of bits to be encoded comprises:

a block of bits received from said multiplexer.

35. (cancelled)

36. (currently amended) An apparatus for reducing decoding complexity, comprising:

a first decoder, wherein said first decoder is configured to:

decode a received frame;

provide a correctly decoded frame; and

provide indication of an erasure if the received frame failed to decode correctly.

a de-multiplexer communicatively coupled to said first decocer;

a plurality of buffers communicatively coupled to said de-multiplexer; and

a plurality of decoders, each of said plurality of decoders being communicatively coupled to one of said plurality of buffers.

37. (currently amended) The apparatus as claimed in claim 35 wherein said de-multiplexer is configured to:

identify a block of bits belonging to [[a]] at least one of the plurality of buffers; and

provide the block of bits to the buffer.

38. (currently amended) The apparatus as claimed in claim 37 wherein said block of bits belonging to [[a]] at least one of the plurality of buffers comprises:

[[a]] the block of bits comprising a frame decoded by said first decoder.

39. (currently amended) The ~~method~~ apparatus as claimed in claim 35 wherein each of said plurality of decoders is configured to:

decode the systematic portion of [[the]] at least one of the plurality of buffers by an outer decoder when the systematic portion is recoverable.

40. (original) The apparatus as claimed in claim 35 wherein each of said plurality of buffers is configured to:

provide systematic portion to higher layers.

41. (original) An apparatus for reducing decoding complexity, comprising:

a plurality of transmit buffers;

a plurality of encoders, each of said plurality of encoders being communicatively coupled to one of said plurality of transmit buffers;

a multiplexer communicatively coupled to said plurality of transmit buffers;

an inner encoder communicatively coupled to said multiplexer;

a first decoder;

a de-multiplexer communicatively coupled to said first decoder;

a plurality of receive buffers communicatively coupled to said de-multiplexer; and

a plurality of decoders, each of said plurality of decoders being communicatively coupled to one of said plurality of receive buffers.

42. (original) The apparatus as claimed in claim 41 wherein each of said plurality of transmit buffers is configured to:

store systematic bits and parity bits.

43. (currently amended) The apparatus as claimed in claim 41 wherein [[each of]] each of said plurality of encoders is configured to:

encode systematic bits to provide parity bits.

44. (original) The apparatus as claimed in claim 43 wherein each of said plurality of encoders is configured to:

encode the systematic bits with a block code.

45. (currently amended) The apparatus as claimed in claim 41 wherein [[each of]] each of said plurality of encoders is configured to:

encode the systematic bits with a Reed-Solomon code.

46. (original) The apparatus claimed in claim 41 wherein said multiplexer is configured to:

provide a block of bits successively from each of said plurality of transmit buffers to said inner encoder.

47. (currently amended) The apparatus as claimed in claim 46 wherein said block of bits comprises a row of [[said]] at least one of the plurality of transmit buffers.

48. (original) The apparatus as claimed in claim 41 wherein said inner encoder is configured to:

identify a block of bits to be encoded; and

encode the block of bits with an inner code.

49. (currently amended) The apparatus as claimed in claim 48 wherein the block of bits to be encoded comprises:

[[a]] the block of bits received from said multiplexer.

50. (currently amended) The ~~method~~ apparatus as claimed in claim 41 wherein said first decoder is configured to:

decode a received frame;

provide a correctly decoded frame; and

provide indication of an erasure if the received frame failed to decode correctly.

51. (currently amended) The apparatus as claimed in claim 41 wherein said de-multiplexer is configured to:

identify a block of bits belonging to [[a]] at least one of the plurality of receive buffers; and

provide the block of bits to the buffer.

52. (currently amended) The apparatus as claimed in claim 51 wherein said block of bits belonging to [[a]] the buffer comprises:

[[a]] the block of bits comprising a frame decoded by said first decoder.

53. (currently amended) The ~~method~~ apparatus as claimed in claim 41 wherein each of said plurality of decoders is configured to:

decode the systematic portion of [[the]] at least one of the plurality of receive buffers by an outer decoder when the systematic portion is recoverable.

54. (currently amended) The apparatus as claimed in claim 41 wherein each of said plurality of buffers is configured to:

provide systematic portion of [[the]] at least one of the plurality of receive buffers to higher layers.